Curriculum Vitae

Name: Ch.Gangadhar

OBJECTIVE

To establish a career in Electronics and Communication engineering that can utilize my knowledge in VLSI Design into technology development

Experience:

16+ years teaching experience (6 years experience as Asst Professor in PVP Siddhartha Institute of Technology+10 years experience as Assoc. Professor in PVP Siddhartha Institute of Technology).

Education:

Doctorate Degree	: **PhD**
Specialization	: **VLSI Design**
University	: **Osmania University**
Post Graduate Degree	:**M.Tech**
Specialization	: **VLSI Design**
College	: **National Institute of Technology ,Warangal**
University	: **National Institute of Technology ,Warangal**
Graduate Degree	:**B.Tech**
Specialization	:**ECE**
College	:**Koneru Lakshmaiah college of engineering.**
University	:**Nagarjuna University, Andhra Pradesh.**

Courses Taught:

- Electronic Devices and Circuits
- Electronic Circuit Analysis
- Basic Electronics
- Digital Electronics
- Object Oriented Programming using C++
- Communication Engineering
- Linear IC Applications
- Digital IC Applications
- Linear and Digital IC Applications
- VLSI Design
- Micro Processors and Multi Core Systems
- Structural Digital Design
- EDC lab
- ECA lab
- Digital Electronics lab
- AC lab

- PDC lab
- ECAD lab
- IC Applications lab

Academic Honors and Awards:

Awarded IETE-KS.Krishnan Memorial Award for the best system oriented paper published by IETE ("Discrete Wavelet Transform and Modified Chaotic Key-Based Algorithm for Image Encryption and Its VLSI Realization", IETE Journal of Research, Vol 58, Issue 2, March-April, 2012).

Research papers:

International Journals

[1] Hyperchaos based image encryption, International Journal of Bifurcation and Chaos,2009

[2] "Discrete Wavelet Transform and Modified Chaotic Key-Based Algorithm for Image Encryption and Its VLSI Realization", IETE Journal of Research, Vol 58, Issue 2, March-April, 2012.

[3] FPGA Implementation of OFDM-Based mmWave Indoor Sparse Channel Estimation Using OMP , Circuits, Systems, and Signal Processing,May,2018

Conferences

[1] "VLSI Realization of Adaptive Equalizers of SIMO FIR Second Order Volterra Channels" , Publsished at IEEE Asia Pacific Conference on Circuits and Systems APCCAS ,December 4-7 ,2006,National University of Singapore ,Singapore.

[2] "Modified chaotic key-based algorithm for image encryption and its VLSI realization" , Proc.IEEE International Conference on Digital Signal Processing (DSP-2007), July 1- 4, 2007, Cardiff University, Wales, U.K.

[3] "VLSI Realization of a Secure Cryptosystem for Image Encryption and Decryption" , Proc.IEEE International Conference on Communications and Signal Processing (ICCSP 2011), 10-12, February 2011, NIT Calicut, Kerala, India.

[4] "Finite Field DWT and MCKBA for Image Encryption and Its VLSI Realization", Proc. 8th IEEE International conference on Information, Communications and Signal

Processing, ICICS 2011, Nanyang Technological University, Singapore, 13-16, December, 2011.

[5] "VLSI Realization of a Secure Filter Bank Based Transmultiplexer for Images using MCKBA and Finite Field Wavelet Packet division Multiplexing" Proc. IEEE Conference, (INDICON 2012), Cochin, India. December 7-9, 2012.

[6] "A Secure Scheme for Multiple Images Transmission and Its VLSI Realization", IETE_GTECT September 28-29, 2013.

[7] FPGA Implementation of 32 Bit Complex Floating Point Multiplier Using Vedic Real Multipliers with Minimum Path Delay 2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering, UPCON 2018.

Workshops Attended:

- A two day workshop **"**MENTOR GRAPHICS BACKEND EDA TOOLS", PVP Siddhartha Institute of Technology from 31-07-2015 to 1-8-2015.
- A five day workshop on "Faculty Enablement Program on Effective Teaching and Assessment Strategies" at VRSEC, Vijayawada, from 16th June, 2014 to 21st June, 2014.
- A Tutorial on "Large-MIMO wireless: Opportunities, Challenges,Solutions" by Prof. A. Chockalingam, Dept of ECE,IISc,Bangalore held at R&T Unit for Navigational Electronics, Osmania University on 26th November,2011.
- Tutorial on "Cognitive Radio A(Biased) Overview" by Dr.Chandra R.Murthy, Dept of ECE.IISc,Bangalore, India held at International Institute of Information Technology(IIIT),Hyderabad on 18th December,2010.
- Tutorial on "Cooperative Communication Systems: Theory and Practice" by Dr. Neelesh B Mehta, Department of ECE IISc, Bangalore held at International Institute of Information Technology(IIIT),Hyderabad on 25th Sept 2010.
- Tutorial on "Services Over IP :Implementation Options and Challenges" by Dr.Bhumip Khasnabish, ZTE, USA Held at R&T unit for Navigational Electronics,Osmania University on 30th July 2010.
- "Faculty Training Program for Effective Communication" organised by Department of Science & Humanities, PVP Siddhartha Institute of Technology during 4-9 May 2009.

- FDP on "System Design Using FPGA" Organised C-DAC ,Hyderabad in collaboration with JNTU, Hyderabad as a part of PREPARE FUTURE project,HRD division Department of Information Technology, Govt of India at C-DAC for a period of two weeks starting from 18-05-2009 to 29-05-2009.

Professional Affiliations:

Member in Indian Society for Technical Education

Primary Skills:

HDL	:	VHDL,Verilog HDL
Tools	:	Xilinx, ModelSim ,Cadence, Synopsys,Altera,Tanner, MS Office.
Operating systems:		Windows
Languages	:	C, C++.