(ELECTIVE – B/I)
4/4 B.Tech. SEVENTH SEMESTER

EE7T5B **VLSI** **Credits: 3**
Lecture: 3 periods/week **Internal assessment: 30 marks**
Tutorial: 1 period /week **Semester end examination: 70 marks**

Course Objectives:

- Understand VLSI Design Flow
- Learn Transistor-Level CMOS Logic Design
- Understand VLSI Fabrication
- Learn to analyze Functionality and Timing Characteristics of Logic Gates

Course Outcomes:

Student will be able to

1. Gain knowledge of different VLSI fabrication processes and CMOS Logic Design.
2. Design different MOS logical circuits.
3. Analyze the effects of Scaling.
4. Program PLDs, CPLDs and FPGAs.

UNIT I

Basic Electrical Properties of MOS Circuits and Fabrication

Introduction to IC Technology, The IC Era, MOS and related VLSI Technology, Basic MOS Transistors. Enhancement and Depletion modes of transistor action, MOS and CMOS Fabrication process, BiCMOS Technology, Comparison between CMOS and Bipolar technologies. Id versus Vds Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor Trans-conductance and Output Conductance, MOS transistor Figure of Merit, The Pass transistor. The nMOS Inverter, The CMOS Inverter, Latch-up.

UNIT II

Layout diagrams: Layout Design rules, Layout Diagrams of CMOS inverter and different logic functions.

Basic Circuit Concepts: Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters,Area Capacitance of Layers, Standard unit of capacitance, Some area Capacitance Calculations, The Delay Unit Inverter Delays, Driving large capacitive loads, Propagation Delays, Wiling Capacitances, Fan-in and fan-out characteristics, Realization of gates using nMOS, pMOS and CMOS technologies.

UNIT III

Scaling of MOS Circuits

Scaling model s and scaling factors, Scaling factors for device parameters, Limitations of scaling, Limits due to sub threshold currents, Limits on logic levels and supply voltage due to noise, Limits due to current density, Introduction to Switch Logic and Gate Logic.

UNIT IV

Programmable Logic Devices (PLDs)

Programmable Logic Arrays (PLA), Programmable Array Logic (PAL). Implementation approaches in VLS1 Design- full Custom Design, Semicustom Design, Gate Arrays, and

Standard Cells,FPGAs

UNIT V

Test Principles

Need for testing, Test Principles, Design Strategies for test, Chip level Test Techniques, System-level Test Techniques.

Learning Resources

Text Books:

1 Essentials of VLSI Circuits and Systems- Kamran Eshraghian, Douglas and APucknell, PHI. Private Limited, 2005.

2 Principles of CMOS VLSI Design - Weste and Eshraghian, Pearson Education, 1999.

Reference Books:

1 Chip Design for Submicron VLSI: CMOS Layout & Simulation, - John P. Uyemura, Thomson Learning,2005.

2 Introduction to VLSI Circuits and Systems - John .P. Uyemura, JohnWiley, 2003.

3 Digital Integrated Circuits - John M. Rabaey, PHI, EEE, 1997.

4 Modern VLSI Design - Wayne Wolf, Pearson Education, 3rd Edition, 1997.

5 VLSI Technology – S.M. SZE, 2nd Edition, TMH, 2003.

6 Fundamentals of Logic Design with VHDL– Stephen. Brown and ZvonkoVranesic, TMH, 2005