IV/IV B. TECH. FIRST SEMESTER
ADVANCED COMPUTER ARCHITECTURE (Elective-I)

Course Code: CS 7T4D **Credits: 3**
Lecture:3 periods/week **Internal assessment: 30 Marks**
Tutorial: 1period/week **Semester end examination: 70 Marks**

Prerequisites: Programming and Data structures, Discrete Maths, and a basic knowledge of Computer organization.

Course Objectives:

1. Understand the Concept of Parallel Processing and its applications.
2. Implement the Hardware for Arithmetic Operations.
3. Analyze the performance of different scalar Computers.
4. Develop the Pipelining Concept for a given set of Instructions.
5. Distinguish the performance of pipelining and non pipelining environment in a processor.

Course Outcomes:

At the end of this course student will:

CO1) Understand the Concept of Parallel Processing and its applications

CO2) Implement the Hardware for Arithmetic Operations

CO3) Analyze the performance of different scalar Computers

CO4) Develop the Pipelining Concept for a given set of Instructions

CO5) Distinguish the performance of pipelining and non pipelining environment in a processor

Syllabus:

UNIT 1
Pipeline and vector processing : Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processors.

UNIT 2
Computer Arithmetic : Addition and Subtraction, Hardware Implementation, Multiplication Algorithms and Hardware Implementation, Division Algorithms and Hardware Implementation, Floating Point Arithmetic Operations.

UNIT 3

Parallel Computer Models : Evolution of Computer Architecture, System Attributes to Performance, Shared Memory Multiprocessors, Distributed Memory Multicomputers, Vector Super Computers, SIMD Super Computers.

UNIT 4

Processors and Memory Hierarchy : Advanced Processor Technology: Design Space of Processors, Instruction-Set Architectures, CISC scalar Processors, RISC scalar Processors, Super Scalar and Vector Processors: Superscalar Processors.

UNIT 5

Pipelining and Superscalar Techniques : Linear Pipeline Processors: Asynchronous and Synchronous models, Clocking and Timing Control, Speedup, Efficiency and Throughput, Pipeline Schedule Optimization, Instruction Pipeline Design: Instruction Execution Phases, Mechanisms for Instruction Pipelining, Dynamic Instruction Scheduling, Branch Handling Techniques.

Learning Resource

Text Books

1. Computer System Architecture, Morris M. Mano, 3rd edition, Pearson/Prentice Hall India.
2. Advanced Computer Architecture, Kai Hwang, McGraw-Hill, India.

References

1.Computer Organization and Achitecture, William Stallings ,8th edition,PHI
2.Computer Organization, Carl Hamachar, Vranesic,Zaky, 5th edition, McGraw Hill.