II/IV B. TECH. SECOND SEMESTER
COMPUTER ORGANIZATION(Required)

Course Code : CS4T5 **Credits: 3**
Lecture: 3 periods/ week **Internal assessment: 30 Marks**
Tutorial: 1period/week **Semester end examination: 70 Marks**

Prerequisites: Digital Logic Design

Course Objectives:

Ability to:

1. Design simple combinational circuits.
2. Design basic building blocks of a computer like ALU, registers, processor and memory at gate level.
3. Analyze the organization of various memory types and I/O devices.
4. Understand the concept of Data Transfer in various components of a computer system.

Course Outcomes:
At the end of this course student will:

CO1) Design simple combinational circuits
CO2) Design basic building blocks of a computer like ALU, registers, processor and memory at gate level.
CO3) Analyze the organization of various memory types and I/O devices.
CO4) Understand the concept of data transfer in various components of a computer system

Syllabus:

UNIT 1

DIGITAL LOGIC CIRCUITS: Digital Computers, Logic Gates, Boolean Algebra: Compliment of a Function, Map Simplification: Product-of-Sums Simplification, Don't-Care Conditions, Combinational Circuits: Half-Adder, Full-Adder, Flip-Flops: SR Flip-Flop, D Flip-Flop, JK Flip-Flop, T Flip-Flop, Edge-Triggered Flip-Flops, Excitation Tables.

UNIT 2

CENTRAL PROCESSING UNIT: General register Organization, Stack Organization: Register Stack, Memory Stack, Reverse Polish Notation, Instruction Formats: Three-Address Instructions, Two-Address Instructions, One-Address Instructions, Zero-Address Instructions ,RISC Instructions, Addressing Modes, Data Transfer and Manipulation, Program Control, Reduced Instruction Set Computer (RISC): CISC Characteristics, RISC Characteristics.

UNIT 3

INPUT-OUTPUT ORGANIZATION: Peripheral Devices: ASCII Alphanumeric Characters, Input-output Interface: I/O Bus and Interface Modules, Asynchronous Data Transfer: Strobe Control, Handshaking, Asynchronous Communication Interface, First-In, First-Out Buffer, Modes of Transfer: Interrupt-Initiated I/O, Priority Interrupt: Daisy-Chaining Priority, Parallel Priority Interrupt, Priority Encoder, Direct Memory Access (DMA): DMA Controller.

UNIT 4

MEMORY ORGANIZATION: Memory Hierarchy, Main Memory: RAM and ROM Chips, Memory Address Map, Memory Connection to CPU, Auxiliary memory: Magnetic Disks, Magnetic Tapes, Associative Memory: Hardware Organization, Match Logic, Read & Write Operations, Cache Memory: Associative Mapping, Direct Mapping, Set-Associative Mapping, Virtual Memory: Address Space and Memory Space, Address Mapping using Pages, Associative Memory Page Table, Page Replacement.

UNIT 5

MULTIPROCESSORS: Characteristics of multiprocessors, Interconnection structures, Inter processor arbitration,Interprocessor communication and synchronization.

Learning Resource

Text Books

1. Computer System Architecture, Morris M. Mano, 3rd edition,Pearson/Prentice Hall India.

References

1. Computer Organization and Achitecture, William Stallings,8th edition,PHI
2. Computer Organization, Carl Hamachar, Vranesic,Zaky, 5th edition, McGraw Hill.