II/IV B. TECH. SECOND SEMESTER
COMPUTER ORGANIZATION LAB(Required)

Course Code : CS 4L3 **Credits: 2**
Lab Hours: 3 periods/ week **Internal assessment: 25 Marks**
Tutorial:- **Semester end examination: 50 Marks**

Prerequisites: Computer Organization

Course Objectives:

1. Understanding the behavior of Logic Gates, Adders, Decoders, Multiplexers and Flip-Flops.
2. Understanding the behavior of ALU, RAM, STACK and PROCESSOR from working modules and the modules designed by the student as part of the experiment.

At the end of this course student will:

CO1) Analyze the behaviour of logic gates
CO2) Design combinational circuits for basic components of computer system and applications.
CO3) Analyze the operational behaviour and applications of various flip-flop
CO4) Design Arithmetic logic units and different types of memory blocks.

Syllabus:

1. Introduction to Verilog HDL/VHDL
2. Verify the behavior of logic gates using truth tables (AND, OR, NOT, XOR, NAND, NOR)
3. Implementing HALF ADDER, FULL ADDER using basic logic gates
4. Implementing Binary -to -Gray, Gray -to -Binary code conversions
5. Implementing 3-8 line DECODER.
6. Implementing 4x1 and 8x1 MULTIPLEXERS.
7. Verify the excitation tables of various FLIP-FLOPS
8. Design of an 8-bit Input/Output system with four 8-bit Internal Registers.
9. Design of an 8-bit ARITHMETIC LOGIC UNIT.

. Design of 24x8 (16 byte) RAM.

. Design of 24x8 (16 byte) STACK.

. Implementation of a 4-bit PROCESSOR.

Learning Resources:

References:

1)A Verilog HDL Primer by J. Bhasker Bk&Hardcover; Published by Star Galaxy Press. ISBN: 0-9656277-4-8

2)Verilog HDL : A Guide to Digital Design and Synthesis by Samir Palnitkar Published by Prentice Hall Publication date: March 1996