

2/4 B.Tech. THIRD SEMESTER**EE3T6****SWITCHING THEORY AND LOGIC DESIGN****Credits: 3****Lecture: 3 periods/week****Internal assessment: 30 marks****Tutorial: 1 period /week****Semester end examination: 70 marks****Course Objectives:**

- To introduce the basic concepts of binary codes, error detecting and correcting codes.
- To study the representation of switching functions using Boolean expressions and their minimization techniques.
- To design and realize various combinational circuits, synchronous and asynchronous sequential logic circuits.
- To analyze various synchronous and asynchronous sequential logic circuits.

Course Outcomes:

Student will be able to

1. Identify the features of various number systems and binary codes.
2. Apply the concepts of Boolean algebra for the analysis & design of various combinational & sequential logic circuits.
3. Design various digital circuits starting from simple ordinary gates to complex programmable logic devices & arrays.
4. Analyze various synchronous and asynchronous sequential circuits.

UNIT I**Number Systems and Binary Codes:**

Philosophy of number systems, complement representation of negative numbers, binary arithmetic, binary codes, error detecting & error correcting codes –Hamming codes.

Boolean algebra: Fundamental postulates of Boolean algebra, Basic theorems and properties.

UNIT II

Switching Functions: Switching functions- Canonical and Standard forms, Algebraic simplification, Digital logic gates, Multilevel NAND/NOR realizations, Minimization of switching functions using K-Map up to 5-variables, Tabulation Method, Prime Implicant chart.

UNIT III

Combinational Logic Circuits: Adders, Subtractors, Parallel Binary Adder, BCD adder, Encoder, Decoder, Multiplexer(MUX), Demultiplexer, MUX Realization of switching functions, Parity generator, Magnitude Comparator, Code converters, PROM, PLA, PAL, Realization of switching functions using PROM,PLA and PAL.

UNIT IV

Sequential Logic Circuits: Classification of sequential circuits (synchronous and asynchronous), Basic flip-flops (NAND RS latch, NOR RS latch, RS flip-flop, JK flip-flop, T flip-flop, D flip-flop with reset and clear terminals), Truth tables and excitation tables, Conversion from one flip-flop to another flip-flop, Design of ripple counters, Design of synchronous counters, Registers, Shift register, Bidirectional Shift register, Universal shift register.

UNIT V

Synchronous Sequential Machines: Finite state machines, Mealy and Moore models, Analysis of Clocked Sequential circuits, Design procedures, State reduction and State assignment, Design and realization of circuits using various Flip-flops.

Learning Resources**Text Book:**

Switching and Finite Automata theory, ZviKohavi and Niraj k Jha, Cambridge University Press, 3rd edition, 2010.

Reference Books:

1. Digital Design, Morris Mano, PHI, 3rd Edition, 2001.
2. Fundamentals of Logic Design, Charles H. Roth, Thomson Publications, 5th Edition, 2009.

Web Resources:

1. <http://www.ece.ubc.ca/~saifz/eece256.htm>
2. http://nptel.iitm.ac.in/courses/Webcoursecontents/IIT%20Guwahati/digital_circuit/frame/index.html