VERILOG HDL

Course Code	20SA8754	**Year**	IV	**Semester**	
Course Category	Skill advanced course	**Branch**	ECE	**Course Type**	LAB
Credits	2	**L-T-P**	1-0-2	**Prerequisites**	Digital Circuits
Continuous Internal Evaluation	0	**Semester End Evaluation**	50	**Total Marks**	50

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Understand the basics of Hardware Description Languages, Program structure and basic language elements of Verilog (L2)
CO2	Analyze various Verilog descriptions for Combinational circuits (L4)
CO3	Simulate arithmetic logic circuits using Verilog (L3)
CO4	Model various Verilog descriptions for Sequential circuits.(L3)
CO5	Make an effective report based on experiments.

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)
Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation
* - Average value indicates course correlation strength with mapped PO

COs	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PSO 1**	**PSO 2**
CO1	1				1								1	
CO2		2			2				2				2	
CO3	1				1				2				1	
CO4	3				3				2				3	
CO5										2				
Average * (Rounded to nearest integer)	2	2			2				2	2			2	

Syllabus		
Expt. No.	**Contents**	**Mapped CO**
Simulate the internal structure of the following Circuits using VERILOG		
I	Verilog Description for all two input basic gates.	CO1
II	Verilog Description for three/four input Logical operations(two experiments)	CO2
III	Verilog Description for Arithmetic operations(Three experiments)	CO3
IV	Verilog Description for multiplexers using dataflow/behavioural method (two experiments)	CO2
V	Verilog Description for flip-flops	CO4
VI	Verilog Description for ripple counters(two experiments)	CO4

VII	Verilog Description for synchronous counters(two experiments)	CO4

- **Minimum 10 experiments to be conducted covering all the topics**

Learning Resources:
Text Books:
1. Samir Palnitkar, Verilog HDL, Pearson Education 2. J. Bhasker, Verilog HDL Synthesis: A Practical Primer
References:
1. Stephen Brown and Zvonko Vranesic - Fundamentals of Digital Logic with Verilog, TMH.
e-Resources:
1.https://nptel.ac.in/courses/106/105/106105165/