LOW POWER VLSI DESIGN

Course Code	20EC6701A	**Year**	IV	**Semester**	I
Course Category	Honors	**Branch**	ECE	**Course Type**	Theory
Credits	4	**L-T-P**	3-1-0	**Prerequisites**	Digital Design
Continuous Internal Evaluation	30	**Semester End Evaluation**	70	**Total Marks**	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Understand the concepts of low power VLSI(L2)
CO2	Apply different circuit techniques to manage the leakage currents(L3)
CO3	Apply the knowledge of architectural approaches. (L3)
CO4	Analyze and Design Low-Voltage Low-Power combinational circuits. (L4)
CO5	Analyze the functionality of Low- voltage low -power memories(L4)

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

* - Average value indicates course correlation strength with mapped PO

COs	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PS O1**	**PS O2**
CO1	2				2					2			2	
CO2	2		2		2					2			2	
CO3	2				2					2			2	
CO4		3			3					3			3	
CO5		2			2					2			2	
Average* (Rounded to nearest integer	2	3	2		2					2			2	

S.NO	**SYLLABUS**	**Mapped COS**
I	**Low power CMOS VLSI design :** Introduction, sources of power dissipation, static power dissipation, active power dissipation. **Circuit techniques for low power design**: Introduction, designing for low power, circuit techniques for leakage power reduction	CO1,CO2
II	**Low-Power Design Approaches:** Low-Power Design through Voltage Scaling: VTCMOS circuits, MTCMOS circuits, Architectural Level Approach-Pipelining and Parallel Processing Approaches	CO1,CO3

III	**Low voltage low power adders**: Introduction, standard adder cells, CMOS adder's architectures, low voltage low power design techniques, current mode adders.	CO1,CO4
IV	**Low voltage low power multipliers**: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier.	CO1,CO4
V	**Low-Voltage Low-Power Memories:** Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.	CO1,CO5

Learning Resources

TEXT BOOK

1. Kiat Seng Yeo, Kaushik Roy (2012), Low Voltage, Low Power VLSI Subsystems, TATA McGraw-Hill
2. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits – Analysis and Design, TMH, 2011.

References:

1. 1.Yeo Rofail,Gohl (2009), CMOS/BiCMOS ULSI Low Voltage, Low Power, Pearson Education Asia 1st Indian reprint.
2. 2.Anantha P. Chandrakasan, Robert W. Brodersen, Low Power Digital CMOS Design, Springer Science
3. 3.Jan M. Rabaey, Anantha P. Chandrakasan, BorivojeNikolic, (2011) Digital Integrated Circuits: a Design Perspective, Pearson Education, 2nd Edition.

e-Resources:

1. 1.https://www.nptelvideos.com/course.php?id=422
2. 2.http://leda.elfak.ni.ac.rs/education/projektovanjeVLSI/predavanja/10%20Low%20Power%20Design%20in%20VLSI.pdf
3. 3.https://www.egr.msu.edu/classes/ece410/salem/files/s16/lectures/Ch2_S2 _N.pdf