Physical Design

course Code	20EC4702C	Year	IV	Semester	I
Course Category	Program Elective-IV	Branch	ECE	Course Type	Theory
Credits	3	L-T-P	3-0-0	Prerequisites	Nil
Continuous Internal Evaluation	30	Semester End Evaluation	70	Total Marks	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Perform IO Design, Floorplan, Power Mesh, Place and Route of a small Design
CO2	Build a clock tree meeting skew and transition requirements
CO3	Understand and fix the timing violations at different stages
CO4	Handle Congestion issues at various stages for a given die size
CO5	Understand the Stick plan and layout of standard cells

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

* - Average value indicates course correlation strength with mapped PO

COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	3	3	2	2	3								3	1
CO2	2	3	2	2	3								3	1
CO3	3	2	2	2	3								3	1
CO4	3	2	2	2	3								3	1
CO5	3	2	2	2	3								3	1
Average* (Rounded to nearest integer)	**3**	**2**	**2**	**2**	**3**								**3**	**1**

Syllabus		
Unit No.	**Contents**	**Mapped CO**
I	**INTRODUCTION TO CMOS CIRCUITS AND LIBRARIES** CMOS circuits – CMOS fabrication process, Transistor Layout, Design rules, Stick diagrams, Spice files, Technology trends. Transistor sizing, Latch-up and its Prevention techniques. **Libraries: -** Technology files, Standard cells, Input-Output pads, library characterization	CO1

II	**SYNTHESIS BASIC AND TIMING CONCEPTS** ASIC Design flow. Verilog Netlist, Basic Synthesis, Design Rule Constraints, Static Timing Analysis(STA) for Timing paths, Clock Uncertainty, Latency, CMOS Inverter: Operation , Delay , Power Dissipation, Wire load models, Corners and its effects on Performance.	CO3
III	**PD(PHYSICAL DESIGN) OVERVIEW & FLOOR-PLANNING** Introduction, Physical Design Flow, Input file for PnR, Floor Planning: Goals & Objectives, Die size estimation, Design Partitioning, I/O Planning and Pad Placement, Floor-plan Considerations Macro Placement, Blockages and Bounds, Power Grid Structure and Power Mesh Implementation.	CO1,CO3
IV	**PLACEMENT AND CLOCK TREE SYNTHESIS** Placement: - Introduction, Goals and Objectives, Placement Phases (Global, Detail), Placement Considerations, Classifications of Placement, Congestion Analysis, Clock Tree Synthesis: - Introduction, Goals and Objectives, Clock Tree Distribution Methodologies, NDR (Non Default Rules).	CO1,CO2
V	**ROUTING, EXTRACTION AND STA** Routing: - Introduction, Goals, and Objectives, Routing Phases (Global Routing, Detail Routing, Search and Repair), Routing Considerations. Extraction: - Introduction, Goals, and Objectives, Standard Parasitic Extraction Format (SPEF). STA: - Timing analysis, Crosstalk Delay.	CO1,CO4,CO5

Learning Resources
Text Books
1.Dan Clein, "CMOS IC Layout - Concepts, Methodologies and Tools", Newnes Publication, 2000. 2.Khosrow Golshan, "Physical Design Essentials - An ASIC Design Implementation Perspective", Springer, 2010.
Reference Books
1.Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison-Wesley Publication, 1999. 2.Neil H.E.Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", Addison-Wesley Publication, 1999. 3.John P. Uyemura, "Physical Design of CMOS ICs", PWS Publishing Company,1995. 4.H. Chang, "Surviving the SOC Revolution", KAP Academic Publishers, 1999.