System Verilog

Course Code	20EC4702B	Year	IV	Semester	I
Course Category	Professional Elective-IV	Branch	ECE	Course Type	Theory
Credits	3	L-T-P	3-0-0	Prerequisites	Nil
Continuous Internal Evaluation:	30	Semester End Evaluation:	70	Total Marks:	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Student should be able to implement basiic assertions using system Verilog(L3)
CO2	Student should be able to develop more complex SVAs using system Verilog(L6)
CO3	Student should be able to develop a UVM testbench with basic features(L6)
CO4	Student should be able to develop a UVM Configuration(L6)

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

* - Average value indicates course correlation strength with mapped PO

COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	3	3	2	2	3								3	1
CO2	2	3	2	2	3								3	1
CO3	3	2	2	2	3								3	1
CO4	3	2	2	2	3								3	1
Average* (Rounded to nearest integer)	**3**	**3**	**2**	**2**	**3**								**3**	**1**

Syllabus		
Unit No.	**Contents**	**Mapped CO**
I	**SVA – I:** Immediate assertions, Concurrent assertions, Implication operators: Overlapped and Non-overlapped, pre-defined functions-$rose,$fell,$stable. Consecutive and non-consecutive repetition operators. Combination of range and repetition operators, disable iff	CO1
II	**SVA – II:** Property blocks, Sequences, Sequence operators, Checkers, parameterized property and sequence blocks, Controlling the assertions.	CO2
III	**UVM TEST BENCH ARCHITECTURE:** Introduction. UVM components , UVM phases and the UVM flow. UVM Factory	CO3,
IV	**UVM METHODOLOGY:** Modeling UVM transactions using Drivers, Monitors, Sequence_items and Sequences. Virtual sequence and sequencer. Component communication through ports	CO3

	and exports.	
V	**UVM CONFIGURATION & COMPONENTS:** UVM Configuration database, UVM Configuration classes, Score boarding, Coverage Monitor, UVM Messaging	CO4

Learning Resources
Text Books
1. Janic Bergeron, "Writing Testbenches: Functional Verification of HDL Models", 2nd Ed., Kluwer Academic Publishers, 2003. 2. Stuart Sutherland, Simon Davidmann and Peter Flake, "System Verilog for Design", 2nd Ed., Springer, 2006. 3. "UVM Cookbook" from Mentor Graphics 4. "Assertions Writing Guide" from Cadence,2016
Reference Books
1. Reference Verification Methodology User Guide, Version 8.5.11 – Synopsis

Physical Design

course Code	20EC4702C	Year	IV	Semester	I
Course Category	Program Elective-IV	Branch	ECE	Course Type	Theory
Credits	3	L-T-P	3-0-0	Prerequisites	Nil
Continuous Internal Evaluation	30	Semester End Evaluation	70	Total Marks	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Perform IO Design, Floorplan, Power Mesh, Place and Route of a small Design
CO2	Build a clock tree meeting skew and transition requirements
CO3	Understand and fix the timing violations at different stages
CO4	Handle Congestion issues at various stages for a given die size
CO5	Understand the Stick plan and layout of standard cells

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

* - Average value indicates course correlation strength with mapped PO

COs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	3	3	2	2	3								3	1
CO2	2	3	2	2	3								3	1
CO3	3	2	2	2	3								3	1
CO4	3	2	2	2	3								3	1
CO5	3	2	2	2	3								3	1
Average* (Rounded to nearest integer)	**3**	**2**	**2**	**2**	**3**								**3**	**1**

Syllabus		
Unit No.	**Contents**	**Mapped CO**
I	**INTRODUCTION TO CMOS CIRCUITS AND LIBRARIES** CMOS circuits – CMOS fabrication process, Transistor Layout, Design rules, Stick diagrams, Spice files, Technology trends. Transistor sizing, Latch-up and its Prevention techniques. **Libraries: -** Technology files, Standard cells, Input-Output pads, library characterization	CO1