

## ADVANCED COMPUTER ARCHITECTURE

<b>Course Code</b>		<b>Year</b>	II	<b>Semester</b>	II
<b>Course Category</b>	<b>Honors</b>	<b>Branch</b>	CSE	<b>Course Type</b>	Theory
<b>Credits</b>	4	<b>L-T-P</b>	4-0-0	<b>Prerequisites</b>	-
<b>Continuous Internal Evaluation :</b>	30	<b>Semester End Evaluation:</b>	70	<b>Total Marks:</b>	100

### COURSE OUTCOMES

Upon successful completion of the course, Student will be able to

<b>CO1</b>	Understand Technological Trends in Computer Architecture	<b>L2</b>
<b>CO2</b>	Apply organizational enhancements to the processor for improving performance.	<b>L3</b>
<b>CO3</b>	Apply Reduced instruction set architecture to optimize pipelining and to enhance instruction level parallelism.	<b>L3</b>
<b>CO4</b>	Analyze parallel processing capabilities of a system.	<b>L4</b>

### Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of correlations (3:Substantial, 2: Moderate, 1:Slight)

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO1	PSO2
<b>CO1</b>														
<b>CO2</b>	3								2	2				3
<b>CO3</b>	3								2	2				3
<b>CO4</b>		3							2	2				3

<b>Syllabus</b>		
<b>Unit No.</b>	<b>Contents</b>	<b>Mapped CO</b>
<b>I</b>	<b>Processor Structure and Function:</b> Processor Organization, Register Organization, The Instruction Cycle, Instruction Pipelining.	<b>CO1, CO2</b>
<b>II</b>	<b>Reduced Instruction Set Computers (RISCs):</b> Instruction Execution Characteristics, The Use of a Large Register File, Compiler-Based Register Optimization, Reduced Instruction Set Architecture, RISC pipelining.	<b>CO1, CO3</b>
<b>III</b>	<b>Instruction-Level Parallelism and Superscalar Processors:</b> Overview, Design Issues , Pentium 4, ARM Cortex-A8.	<b>CO1, CO3</b>
<b>IV</b>	<b>Parallel Processing:</b> The Use of Multiple Processors, Symmetric Multiprocessors, Cache Coherence and the MESI Protocol, Multithreading and Chip Multiprocessors, Clusters, Nonuniform Memory Access Computers.	<b>CO1, CO4</b>
<b>V</b>	<b>Multicore Computers:</b> Hardware Performance Issues, Software Performance Issues, Multicore Organization, Intel x86 Multicore Organization.ARM11 MPCore.	<b>CO1, CO4</b>

<b>Learning Resources</b>
<b>Text Books</b>
1. “Computer Organization and Architecture- Design for performance”, William Stallings, Pearson Education, Eighth Edition, 2013.
<b>References</b>
1. “Computer Architecture - A Quantitative Approach”, John L. Hennessy and David A. Patterson, Morgan Kaufmann/Elsevier, Fifth edition, 2012.
2. “Advanced Computer Architecture”, Kai Hwang, Tata McGraw-Hill Education, Second Edition, 2013.
<b>e- Resources &amp; other digital material</b>
1. <a href="https://nptel.ac.in/courses/106103206">https://nptel.ac.in/courses/106103206</a>
2. <a href="https://nptel.ac.in/courses/106102229">https://nptel.ac.in/courses/106102229</a>