PVP-19

INTRODUCTION TO VLSI DESIGN

Course Code	19EC3602	**Year**	III	**Semester**	II
Course Category	Program Core	**Branch**	ECE	**Course Type**	Theory
Credits	3	**L-T-P**	3-0-0	**Prerequisites**	Nil
Continuous Internal Evaluation:	30	**Semester End Evaluation:**	70	**Total Marks:**	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Analyze and simulate Verilog modules (L4)
CO2	Program PLDs, CPLDs and FPGAs. (L4)
CO3	Analyze VLSI fabrication processes and CMOS Logic Design (L4).
CO4	Compare different scaling methods of MOS logical circuits and subsystems. (L2)

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

* - Average value indicates course correlation strength with mapped PO

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3		3		3					3			3	
CO2	3		3		3					3			3	
CO3	3	3								3			3	
CO4	3	3								3			3	
Average* (Rounded to nearest integer)	3	3	3	3	3					3			3	

Syllabus

Unit No.	**Contents**	**Mapped CO**
I	**Computer-Aided Design:** Hardware Description Languages, Verilog Description of Combinational Circuits, Verilog Modules, Verilog Assignments, Procedural Assignments, Modelling Flip-Flops Using Always Block, Delays in Verilog, Compilation, Simulation, and Synthesis of Verilog Code, Verilog Data Types and Operators, Simple Synthesis Examples, Verilog Models for Multiplexers, Modeling Registers, Counters and finite state machines using Verilog Always Statements, Behavioural and Structural Verilog, Testing a Verilog Model.	CO1
II	**Programmable Logic Devices: Complex** Programmable Logic Devices (CPLDs), Field-Programmable Gate Arrays (FPGAs), Implementing Functions in FPGAs.	CO2
III	**IC Design Technology:** Integrated Circuit (IC) Era, Metal-Oxide-semiconductor (MOS) and related VLSI technology, basic MOS transistors, enhancement mode transistor action, NMOS fabrication, CMOS fabrication, comparison of NMOS, CMOS, BICMOS, GaAs technologies.	CO3

IV	**Electrical Properties of MOS circuits:** Drain current vs Drain-Source voltage relationships, MOS transistor threshold voltage, pass transistor, NMOS inverter, CMOS inverter. **MOS Circuit Design Process:** MOS Layers, Stick Diagrams, Design Rules and Layout, 2µm micron based design rules. Layout Diagrams	CO3
V	**Scaling of MOS Circuits:** Scaling Models and Scaling factors, Scaling factors for device parameters, Limits of scaling **Subsystem Design:** Some architectural issues, Switch Logic, Gate Logic, Examples of structured design, parity generator, multiplexers	CO3,CO4

Learning Resources
Text Books
1. Charles H. Roth, Lizy Kurian John, Byeong Kil Lee, Digital Systems Design using Verilog, 1/e, Cengage Learning, 2016. 2. Douglas A, Pucknell, Kamran Eshraghian, Essentials of VLSI Circuits and Systems, 1/e, Prentice Hall, 2012
References
1. Kang, Leblibici, CMOS Digital Integrated Circuits, 3/e, Tata McGraw Hill, 2001. 2. Jan M. Rabaey, Digital Integrated Circuits, 2/e, Pearson Education, 2002. 3. Jackson, Hodges, Analysis and Design of Digital Integrated Circuits, 3/e, Tata McGraw Hill, 2010. 4. Gary S May, Simon M Sze, Fundamentals of Semiconductor Fabrication, 1/e, Wiley, 2004.
e-Resources
1. https://nptel.ac.in/courses/108/107/108107129/ 2. https://www.cin.ufpe.br/~mel/pub/prototipac%E3o/referencias/CMOS_design/CMOS-VLSI-design.pdf